1   <u>CLAIMS</u>

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3   What is claimed is:

4   1.   A digital clock manager having a reference input

5   terminal, a skew input terminal, an output terminal, and a

6   frequency adjusted output terminal, the digital clock

7   manager comprising:

8   a delay lock loop (DLL) coupled to the reference

9   input terminal, the skew input terminal, and the output

10   terminal; and

11   a digital frequency synthesizer, coupled to the

12   delay lock loop and the frequency adjusted output

13   terminal.

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15   2.   The digital clock manager of Claim 1, wherein the

16   delay lock loop is configured to generate an output clock

17   signal on the output terminal which synchronizes a reference

18   clock signal on the reference input terminal with a skewed

19   clock signal on the skew input terminal.

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21   3.   The digital clock manager of Claim 1, wherein the

22   digital frequency synthesizer is configured to generate a

23   frequency adjusted clock signal on the frequency adjusted

24   output terminal and wherein the frequency adjusted clock

25   signal is synchronized with the output clock signal during

26   concurrences.

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28   4.   The digital clock manager of Claim 1, wherein the

29   delay lock loop comprises a DLL output circuit having a DLL

30   output delay.

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32   5.   The digital clock manager of Claim 4, wherein the

33   digital frequency synthesizer comprises a DFS output circuit

34   having a DFS output delay.

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6.   The digital clock manager of Claim 5, wherein the DLL output delay is substantially equal to the DFS output delay.

7.   The digital clock manager of Claim 5, wherein the DLL output circuit comprises a plurality of components and the DFS output circuit comprises the same plurality of components.

8.   The digital clock manager of Claim 1, wherein the delay lock loop drives a synchronizing clock signal to the digital frequency synthesizer.

9.   The digital clock manager of Claim 8, wherein the delay lock loop is configured to generate an output clock signal on the output terminal, wherein the output clock signal lags the synchronizing clock signal by a DLL output delay.

10.   The digital clock manager of Claim 9, wherein the digital frequency synthesizer is configured to generate a frequency adjusted clock signal on the frequency adjusted output terminal, wherein an active edge of the frequency adjusted clock signal lags an active edge of the synchronizing clock signal by a DFS output delay during a concurrence period.

11.   The digital clock manager of Claim 10, wherein the DLL output delay is substantially equal to the DFS output delay.

12.   The digital clock manager of Claim 1, further comprising a variable delay circuit coupled between the delay lock loop and the output terminal.

1   13.   The digital clock manager of Claim 1, further
2   comprising a variable delay circuit coupled between the
3   digital frequency synthesizer and the frequency adjusted
4   output terminal.

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6   14.   The digital clock manager of Claim 1, further
7   comprising a multiplexer having a first input terminal
8   coupled to the reference input terminal, a second input
9   terminal coupled to the delay lock loop, and an output
10 terminal coupled to the digital frequency synthesizer.

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12   15.   The digital clock manager of Claim 1, wherein the
13 delay lock loop is configured to provide a synchronizing
14 clock signal to the second input terminal of the
15 multiplexer.

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17   16.   The digital clock manager of Claim 15, wherein the
18 digital frequency synthesizer is configured to perform a
19 frequency search phase using a reference clock signal
20 provided to the reference input terminal.

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22   17.   The digital clock manager of Claim 16, wherein the
23 digital frequency synthesizer is configured to provide a
24 frequency adjusted clock signal based on the synchronizing
25 clock signal.

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27   18.   The digital clock manager of Claim 1, wherein the
28 digital frequency synthesizer performs a frequency search
29 while the delay lock loop is performing lock acquisition.

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31   19.   A method to generate an output clock signal and a
32 frequency adjusted clock signal from a reference signal,
33 wherein the output clock signal is synchronized with the
34 frequency adjusted clock signal during a concurrence; the
35 method comprising:
36   generating a synchronizing clock signal;

1   matching a DLL output delay with a DFS output
2   delay;
3   generating the output clock signal lagging the
4   synchronizing clock signal by the DLL output delay; and
5   generating the frequency adjusted clock signal so
6   that an active edge of the frequency adjusted clock
7   signal lags an active edge of the synchronizing clock
8   signal by the DFS output delay during the concurrence.
9
10   20.   The method of Claim 19, wherein the step of
11   matching a DLL output delay with a DFS output delay
12   comprises synchronizing a DLL output circuit with a DFS
13   output circuit.
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15   21.   The method of Claim 19, further comprising
16   performing lock acquisition.
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18   22.   The method of Claim 21, further comprising
19   performing a frequency search during lock acquisition.